# HARRISH RAJPUT

## PROFILE

ASIC Design & Implementation Engineer.

## EXPERIENCE

TECHNICAL STAFF, AMD; CANADA – JAN 2015 - AUG 2015

CONSULTANT ASIC, QUALCOMM; CANADA – 2013 - 2015

STAFF/BUSINESS PARTNER, TRAJECTORY , CANADA – 2011 - 2012

TEAM LEAD, INFINEON; INDIA/GERMANY – 2006 - 2009

ASIC ENGINEER, SASKEN/TEXAS INSTRUMENTS; INDIA – 2005 - 2006

PROJECT TRAINEE, CDAC; INDIA – 2004 - 2006

## EDUCATION

UNIVERSITY OF BRITISH COLUMBIA, CANADA – PHD (DOCTORAL CANDIDATE)
DROP OUT ( ELECTRICAL ENGINEERING 2012, FINANCE 2015)

UNIVERSITY OF BRITISH COLUMBIA, CANADA – MASC (ELECTRICAL ENG 2011)

CDAC, INDIA – MTECH (VLSI 2005)

INTEGRAL UNIVERSITY, INDIA – BTECH (COMPUTER ENG 2002)

## PATENTS

H.Rajput, A. Labun, T. Johnson, "Method and systems for estimating a diffusion potential of a diffusive property", US WO2012135948 A1.

## PUBLICATIONS

H. Rajput, A. Milani, A. Labun, "Including time dependancy and ANOVA in decision making using the revised fuzzy AHP: a case study on wafer fabrication process selection", Applied Soft Computing, Elsevier, 2011, 11, 5099-5109.

Balagopal, H. Rajput, C. Kypa, H. Iking, V. Costa, "DFT Concepts for physical layers", Infineon tech conference, Singapur 2007.

Last edited: May 2016

Toronto | Ottawa, Canada 647-274-0000 youtube.com/Leprofesseur